## Amendment to the Specification

### Abstract

Please replace the abstract with the following:

A pipelined fast Fourier transform (FFT) processor for receiving an input sequence, that has at least one FFT triplet module having first, second and third butterfly modules connected in series by selectable multipliers for selectively performing trivial coefficient multiplication and complex coefficient multiplication on output data sequences of adjacent butterfly modules. The FFT processor also has a selectable multiplier that is selected in response to a control signal provided with each butterfly module. The control signal can have a combination of a current and prior switching signal. In one embodiment each of the at least one FFT triplet modules terminate in a twiddle factor multiplier for applying a twiddle factor to an output of the third butterfly module of the respective triplet module. Also the at least one FFT triplet module can receive an input sequence and for outputting a final output data sequence representing an FFT of the input sequence.

### Detailed Description

Please amend paragraph 45 as follows:

FIG. 12 illustrates an exemplary pre-multiplication radix-2 butterfly unit 170 through the illustration of its logical layout. The operation of this exemplary pre-multiplication butterfly unit 170 corresponds to the method of the butterfly operation described above. As before, one skilled in the art will understand the implementation of this exemplary butterfly on any number of platforms. Node 172 receives the real component of the n.sup.th sample, x.sub.r(n), while node 176 receives x.sub.i(n), the imaginary component of the n.sup.th sample. Nodes 180 and 184 receive the real and imaginary components of the (n+N/2).sup.th sample, x.sub.r(n+N/2) and x.sub.i(n+N/2), as determined by a control signal. The control signal also determines the application of a real-imaginary swap to the values at those nodes prior to their arrival at an adder. The control signal is provided by a logical AND gate 188 receiving as its input switching signals [~~S.sub.n9-1~~] S.sub.n-1, and S.sub.n. S.sub.n is also used to switch between values

after the adder, as will be described below. Adder 174 sums the value at nodes 172 and 180, and forwards the sum to node 172a. Adder 178 sums the value at nodes 176 with the value at node 184 or the negative of the value at node 184, as determined by the control signal of 188. The sum or difference of the values is forwarded to node 176a. Adder 182 sums the value of node 172 and the negative value of node 180 to obtain the difference in the values at the two nodes. The difference in the values is forwarded to node 180a. Adder 186 sums the value of node 176 with the value of node 184 or the negative of the value at node 184, as determined by the control signal of 188. The sum or difference of the values is forwarded to node 184a. One skilled in the art will appreciate that adder 182 functions as a subtractor and adders 178 and 186 with their respective premultiplication by -j function as adder-subtractor blocks and can be implemented without departing from the present invention. The output of the butterfly unit 170 is controlled by synchronization signal S.sub.n which controls a switch at each output. X.sub.r(n) is determined in accordance with the switching signal, as described above, to select between the values at nodes 172 and 172a. X.sub.i(n) is determined in accordance with the switching signal, as described above, to select between the values at nodes 176 and 176a. X.sub.r(n+N/2) is determined in accordance with the switching signal, as described above, to select between the values at nodes 180 and 180a. X.sub.i(n+N/2) is determined in accordance with the switching signal, as described above, to select between the values at nodes 184 and 184a. One skilled in the art will appreciate that the pre-multiplication performed by this butterfly unit is selectively applied and allows the integration of a selective trivial multiplication with an adjacent butterfly unit which can offer advantages in terms of implementation size and complexity.